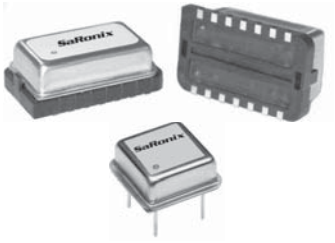
查询S131供应商

SaRonix

Voltage Controlled Crystal Oscillator 3.3 & 5V, LVCMOS/LVTTL

Technical Data

Sx1310 / Sx1319 / Sx1510 / Sx1519 Series



ACTUAL SIZE

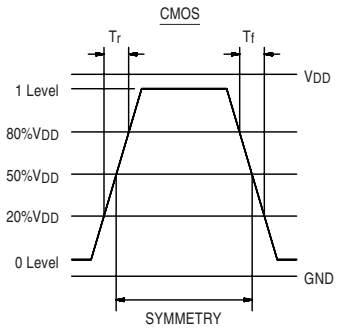
Description

A voltage controlled crystal oscillator with a wide range of performance options to 125 MHz. The devices are packaged in either standard 14-pin or 8-pin DIP compatible all metal, resistance welded packages for commercial or industrial temperature range applications. True SMD DIL14 versions for IR reflow are available, select option "S" in part number builder. See separate data sheet for SMD package dimensions.

Applications & Features

- Phase-locked loops encountered in Telecom, LAN and Wireless data, and in video processing applications
- LVCMOS, LVTTL compatible
- ˜ Tri-state option available

Output Waveform



Frequency Range:	32 MHz to 125 MHz
Frequency Stability:	±25 or ±50 ppm over all conditions: operating temperature, voltage change, load change, calibration tolerance, with V_C = 2.5V @ 5V, VC = 1.65V @ 3.3V
Aging:	@ 40°C: ±10 ppm max for 5 years or ±12 ppm max for 10 years
Temperature Range:	
Operating:	0 to +70°C or -40 to +85°C
Storage:	-55 to +125°C
Supply Voltage:	
Recommended Operating:	5V ±5% or 3.3V ±10%
Supply Current:	
32 to 70 MHz:	50mA max, 35mA max @ 3.3V
70+ to 125 MHz:	65mA max, 35mA max @ 3.3V
Output Drive:	
Symmetry:	3.3V: 45/55% max @ 50% V_{DD} for 0 to 70°C, 3.3V: 40/60% max @ 50% V_{DD} for -40 to +85°C 5.0V: 45/55% max @ 50% V_{DD} or 40/60% max @ 1.4V TTL level
Rise & Fall Times:	4ns max: 20% to 80% V_{DD} 1.5ns max: 0.5V to 2.5V @ 5V TTL only
Logic 0:	0.5V max @ 5V or 20% V_{DD} max @ 3.3V
Logic 1:	2.5V min @ 5V or 80% V_{DD} min @ 3.3V
Load:	5V: 5TTL or 50pF, 32 to 50 MHz 5V: 5TTL or 30pF 50+ to 125 MHz 3.3V: 30pF up to 80 MHz, 95Ω AC up to 125 MHz
Jitter:	20ps max RMS period jitter
Pull Characteristics:	
Input Impedance:	50KΩ min
Frequency Response (-3dB):	50 kHz min
Pullability:	±25, ±50, ±75, ±100 ppm APR*
Control Voltage:	0.5 to 4.5V @ 5V or 0.3 to 3.0V @ 3.3V
Transfer Function:	Frequency increases when Control Voltage increases
Linearity:	5% or 10% max
Center Control Voltage:	2.5V @ 5V, 1.65V @ 3.3V
Phase noise:	-95 dbc typ / Hz @ 100Hz -110 dbc typ / Hz @ 1kHz -100 dbc typ / Hz @ 10kHz
Mechanical:	
Shock:	MIL-STD-883, Method 2002, Condition B
Solderability:	MIL-STD-883, Method 2003
Terminal Strength:	MIL-STD-202, Method 211, Conditions B2
Vibration:	MIL-STD-883, Method 2007, Condition A
Solvent Resistance:	MIL-STD-202, Method 215
Resistance to Soldering Heat:	MIL-STD-202, Method 210, Condition A, B or C (I or J for Gull Wing)
Environmental:	
Gross Leak Test:	MIL-STD-883, Method 1014, Condition C
Fine Leak Test:	MIL-STD-883, Method 1014, Condition A2
Thermal Shock:	MIL-STD-883, Method 1011, Condition A
Moisture Resistance:	MIL-STD-883, Method 1004

* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability)
NOTE: APR is inclusive of Aging

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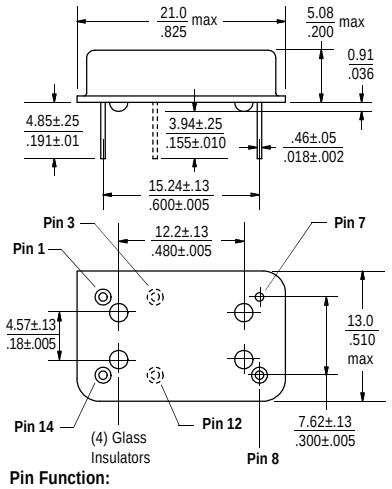
Package Details

FULL SIZE PACKAGE

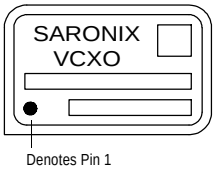


Pin Function:

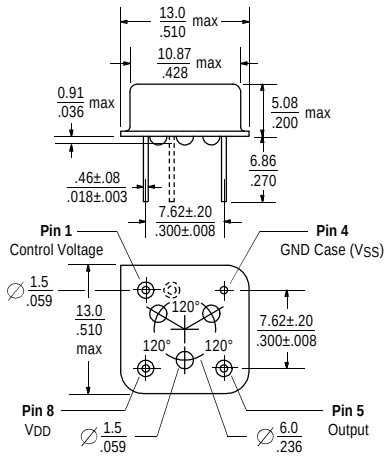
Pin 1: Control Voltage
Pin 3: Tri-State control (Tri-State version only)
Pin 7: GND / Case (V_{SS})
Pin 8: Output
Pin 12: N/C (Tri-State version only)
Pin 14: VDC (V_{DD})

Standard Marking Format

Includes Date Code, Frequency & Part Number



HALF SIZE PACKAGE



Standard Marking Format

Includes Date Code, Frequency & Part Number

Scale: None (Dimensions in $\frac{mm}{inches}$)

Part Numbering Guide

S T 151 0 B A B J - 60.0000 (T)

SaRonix

T = Tri-State
Blank = Non Tri-State

Series
131 = 3.3V
151 = 5.0V

Package Size
0 = Full Size
9 = Half Size

Stability Tolerance
A = ±25 ppm, 0 to 70°C
B = ±50 ppm, 0 to 70°C
E = ±50 ppm, -40 to +85°C

Pullability (min APR*)
A = ±50 ppm
B = ±100 ppm
G = ±25 ppm
H = ±75 ppm

Linearity
A = 5%
B = 10%

Lead Style
Blank = Thru-Hole
J = Gull Wing
S = True SMD Adaptor for Full Size packages, see separate data sheet for dimensions

Packing Method
(T) = Tape & Reel for SMD versions, full reel increments only, 200pcs (full size) or 250pcs (half size)
Blank = Bulk

Frequency (MHz)

* APR = (VCXO Pull relative to specified Output Frequency) – (VCXO Frequency Stability)
NOTE: APR is inclusive of Aging

Tri-State Logic Table

Pin 3 Input	Pin 8 Output
Logic 1 or NC	Oscillation
Logic 0 or GND	High Impedance

Required Input Levels on Pin 3:
Logic 1 = 3.0V min
Logic 0 = 0.3V max

Test Circuits

Figure 1
30pF or 50pF Load

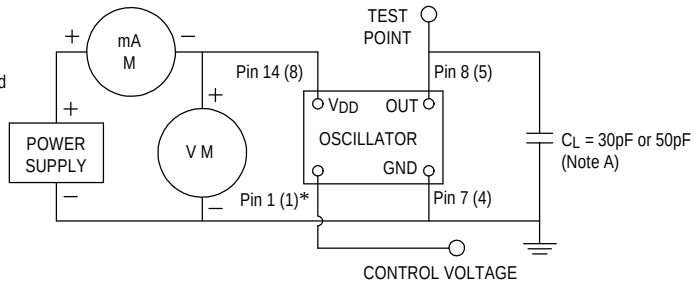
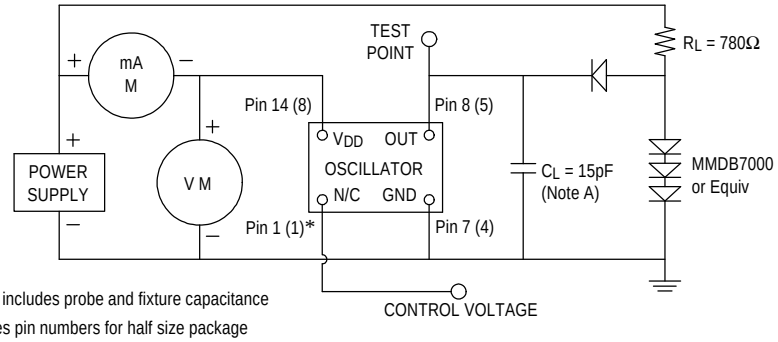


Figure 2
TTL Load



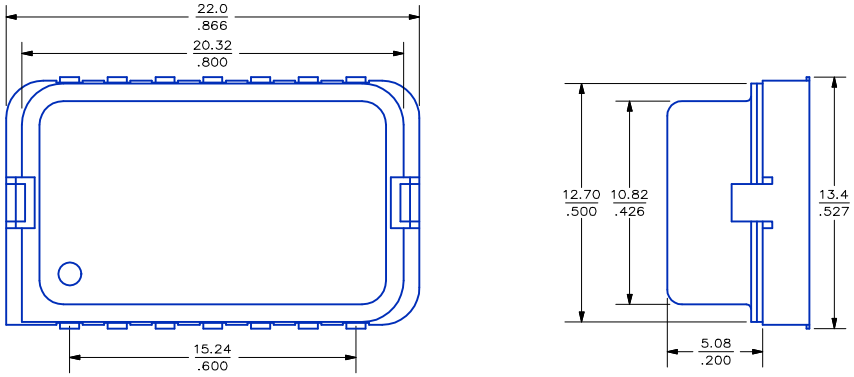
NOTE A: CL includes probe and fixture capacitance
*( ) Indicates pin numbers for half size package

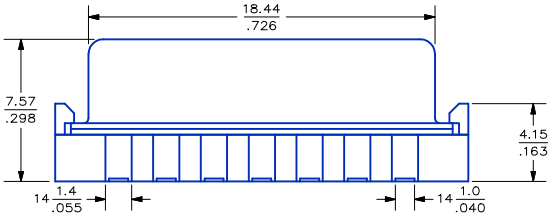
All specifications are subject to change without notice.

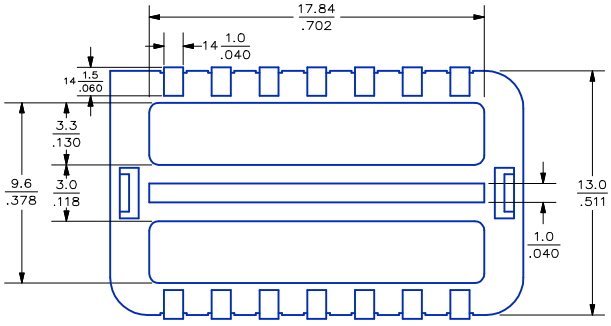
DS-162 REV E

True SMD Adaptor - 7.57mm High

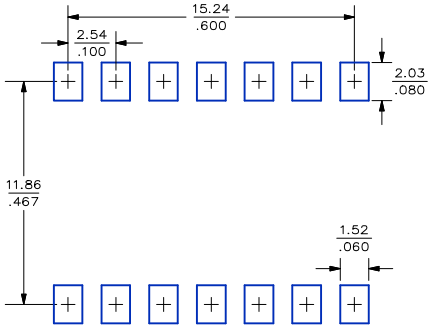
Technical Data







RECOMMENDED LAND PATTERN



REV A